

Study of Common Emitter Transistor Amplifier circuit

Objectives:

1. To design a common emitter transistor (NPN) amplifier circuit.
2. To obtain the frequency response curve of the amplifier and to determine the mid-frequency gain, A_{mid} , lower and higher cutoff frequency of the amplifier circuit.

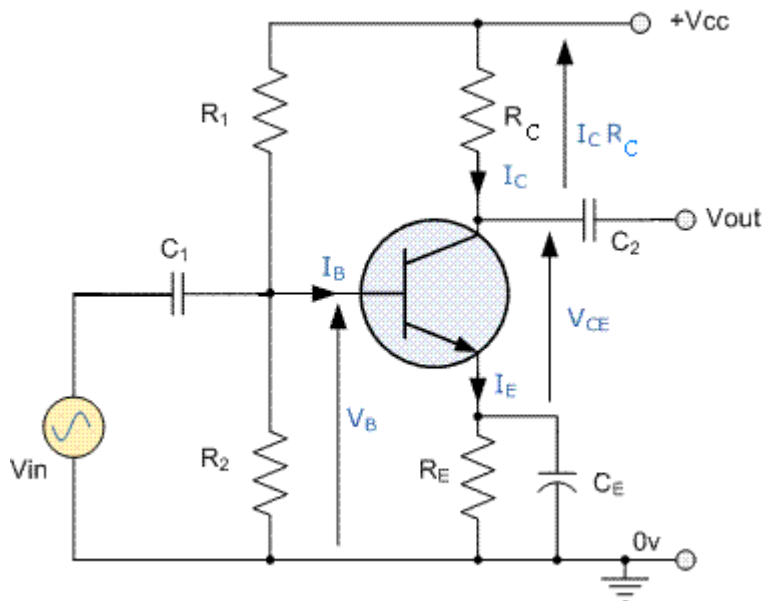
Overview:

The most common circuit configuration for an NPN transistor is that of the *Common Emitter Amplifier* and that a family of curves known commonly as the *Output Characteristics Curves*, relates the Collector current (I_C), to the output or Collector voltage (V_{CE}), for different values of Base current (I_B). All types of transistor amplifiers operate using AC signal inputs which alternate between a positive value and a negative value. Presetting the amplifier circuit to operate between these two maximum or peak values is achieved using a process known as *Biasing*. Biasing is very important in amplifier design as it establishes the correct operating point of the transistor amplifier ready to receive signals, thereby reducing any distortion to the output signal.

The single stage common emitter amplifier circuit shown below uses what is commonly called "Voltage Divider Biasing". The Base voltage (V_B) can be easily calculated using the simple voltage divider formula below:

$$V_B = \frac{V_{CC}R_2}{R_1 + R_2}$$

Thus the base voltage is fixed by biasing and independent of base current provided the current in the divider circuit is large compared to the base current. Thus assuming $I_B \approx 0$, one can do the approximate analysis of the voltage divider network without using the transistor gain, β , in



the calculation. Note that the approximate approach can be applied with a high degree of accuracy when the following condition is satisfied:

$$\beta R_E \geq 10R_2$$

Load line and Q-point

A static or DC load line can be drawn onto the output characteristics curves of the transistor to show all the possible operating points of the transistor from fully "ON" ($I_C = V_{CC}/(R_C + R_E)$) to fully "OFF" ($I_C = 0$). The quiescent operating point or **Q-point** is a point on this load line which represents the values of I_C and V_{CE} that exist in the circuit when no input signal is applied. Knowing V_B , I_C and V_{CE} can be calculated to locate the operating point of the circuit as follows:

$$V_E = V_B - V_{BE}$$

So, the emitter current,

$$I_E \approx I_C = \frac{V_E}{R_E}$$

$$\text{and } V_{CE} = V_{CC} - I_C(R_C + R_E)$$

It can be noted here that the sequence of calculation does not need the knowledge of β and I_B is not calculated. So the Q-point is stable against any replacement of the transistor.

Since the aim of any small signal amplifier is to generate an amplified input signal at the output with minimum distortion possible, the best position for this Q-point is as close to the centre position of the load line as reasonably possible, thereby producing a Class A type amplifier operation, i.e. $V_{CE} = 1/2V_{CC}$.

Coupling and Bypass Capacitors

In CE amplifier circuits, capacitors C_1 and C_2 are used as Coupling Capacitors to separate the AC signals from the DC biasing voltage. The capacitors will only pass AC signals and block any DC component. Thus they allow coupling of the AC signal into an amplifier stage without disturbing its Q point. The output AC signal is then superimposed on the biasing of the following stages. Also a bypass capacitor, C_E is included in the Emitter leg circuit. This capacitor is an open circuit component for DC bias, meaning that the biasing currents and voltages are not affected by the addition of the capacitor maintaining a good Q-point stability. However, this bypass capacitor acts as a short circuit path across the emitter resistor at high frequency signals increasing the voltage gain to its maximum. Generally, the value of the bypass capacitor, C_E is chosen to provide a reactance of at most, 1/10th the value of R_E at the lowest operating signal frequency.

Amplifier Operation

Once the Q-point is fixed through DC bias, an AC signal is applied at the input using coupling capacitor C_1 . During positive half cycle of the signal V_{BE} increases leading to increased I_B . Therefore I_C increases by β times leading to decrease in the output voltage, V_{CE} . Thus the CE amplifier produces an amplified output with a phase reversal. The voltage Gain of the common emitter amplifier is equal to the ratio of the change in the output voltage to the change in the input voltage. Thus,

$$A_V = \frac{V_{out}}{V_{in}} = \frac{\Delta V_{CE}}{\Delta V_{BE}}$$

The input (Z_i) and output (Z_o) impedances of the circuit can be computed for the case when the emitter resistor R_E is completely bypassed by the capacitor, C_E :

$$Z_i = R_1 \parallel R_2 \parallel \beta r_e \text{ and } Z_o = R_C \parallel r_o$$

where r_e ($26\text{mV}/I_E$) and r_o are the emitter diode resistance and output dynamic resistance (can be determined from output characteristics of transistor). Usually $r_o \geq 10 R_C$, thus the gain can be approximated as

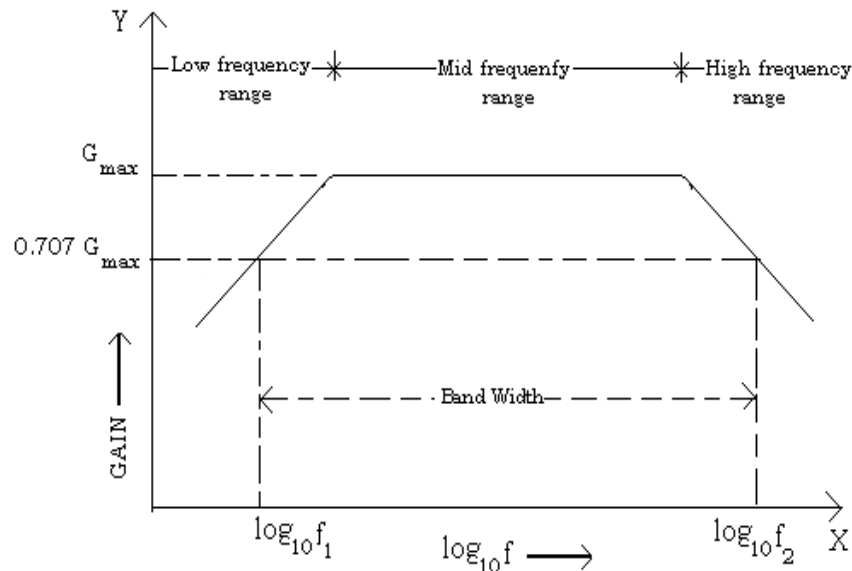
$$A_V = \frac{V_{\text{out}}}{V_{\text{in}}} = -\frac{\beta I_B (R_C \parallel r_o)}{I_B \beta r_e} \approx -\frac{R_C}{r_e}$$

The negative sign accounts for the phase reversal at the output. In the circuit diagram provided below, the emitter resistor is split into two in order to reduce the gain to avoid distortion. So the expression for gain is modified as

$$A_V \approx -\frac{R_C}{(R_{E1} + r_e)}$$

Frequency Response Curve

The performance of an amplifier is characterized by its frequency response curve that shows output amplitude (or, more often, voltage gain) plotted versus frequency (often in log scale). Typical plot of the voltage gain of an amplifier versus frequency is shown in the figure below. The frequency response of an amplifier can be divided into three frequency ranges.



The frequency response begins with the lower frequency range designated between 0 Hz and lower cutoff frequency. At lower cutoff frequency, f_L , the gain is equal to $0.707 A_{\text{mid}}$. A_{mid} is a constant mid-band gain obtained from the mid-frequency range. The third, the higher frequency range covers frequency between upper cutoff frequency and above. Similarly, at higher cutoff frequency, f_H , the gain is equal to $0.707 A_{\text{mid}}$. Beyond this the gain decreases with frequency increases and dies off eventually.

The Lower Frequency Range

Since the impedance of coupling capacitors increases as frequency decreases, the voltage gain of a BJT amplifier decreases as frequency decreases. At very low frequencies, the capacitive reactance of the coupling capacitors may become large enough to drop some of the input voltage or output voltage. Also, the emitter-bypass capacitor may become large enough so that it no longer shorts the emitter resistor to ground.

The Higher Frequency Range

The capacitive reactance of a capacitor decreases as frequency increases. This can lead to problems for amplifiers used for high-frequency amplification. The ultimate high cutoff frequency of an amplifier is determined by the physical capacitances associated with every component and of the physical wiring. Transistors have internal capacitances that shunt signal paths thus reducing the gain. The high cutoff frequency is related to a shunt time constant formed by resistances and capacitances associated with a node.

Design:

Before designing the circuit, one needs to know the circuit requirement or specifications. The circuit is normally biased for V_{CE} at the mid-point of load line with a specified collector current. Also, one needs to know the value of supply voltage V_{CC} and the range of β for the transistor being used (available in the datasheet of the transistor).

Here the following specifications are used to design the amplifier:

$V_{CC} = 12V$ and $I_C = 1 mA$

Start by making $V_E = 0.1 V_{CC}$. Then $R_E = V_E / I_E$ (Use $I_E \approx I_C$).

Since $V_{CE} = 0.5 V_{CC}$, Voltage across $R_C = 0.4 V_{CC}$, i.e. $R_C = 4.R_E$

In order that the approximation analysis can be applied, $R_2 \leq 0.1\beta R_E$. Here β is the minimum rated value in the specified range provided by the datasheet (in this case $\beta=50$).

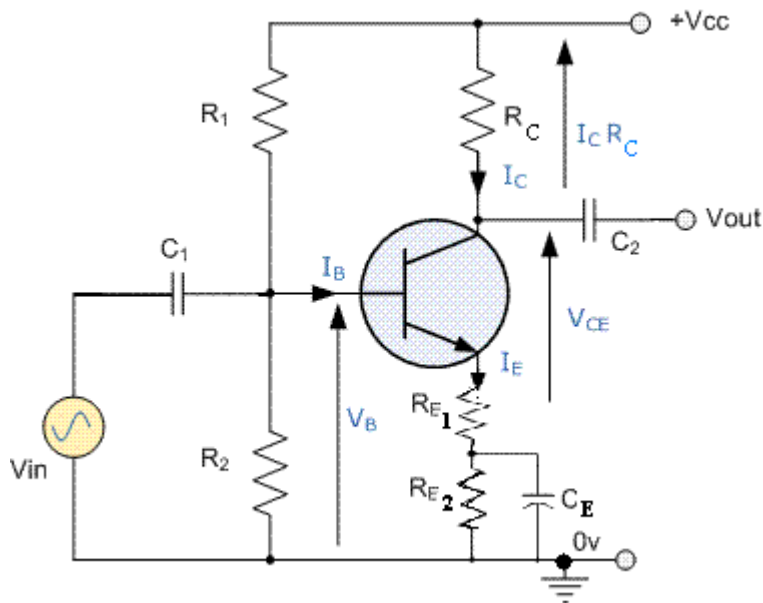
Finally, $R_1 = \frac{V_1}{V_2} R_2$, $V_1 (= V_{CC} - V_2)$ and $V_2 (= V_E + V_{BE})$ are voltages across R_1 and R_2 , respectively.

Based on these guidelines the components are estimated and the nearest commercially available values are used.

Components/ Equipments:

1. Transistor: CL100 (or equivalent general purpose npn)
2. Resistors: $R_1 = 26 (27) K\Omega$, $R_2 = 5 (4.7+0.22) K\Omega$, $R_C = 4 (3.9) K\Omega$, $R_E = 1k\Omega$ ($R_{E1}=470 \Omega$, $R_{E2}=560 \Omega$)
3. Capacitors: $C_1 = C_2 = 1 \mu F$ (2 nos.), $C_E = 100\mu F$
4. Power Supply ($V_{CC} = 12V$)
5. Oscilloscope
6. Function Generator (~ 100-200 mV pp, sinusoidal for input signal)
7. Breadboard
8. Connecting wires

Circuit Diagram:



Procedure:

1. Measure and record all the values of resistance and capacitance and β of the transistor using a multimeter. Configure the circuit as per the diagram.
2. Apply supply voltage to the circuit. Measure and record all the dc parameters listed in Table 1 in absence of the ac signal.
3. Next, set the function generator in 20Hz “Frequency” range. Also, set the “Attenuation” button at 40dB. Connect the output to the oscilloscope and adjust the “Amplitude” knob till you get a sinusoidal input signal, $V_i \approx 100\text{-}200$ mV peak-to-peak value. **DO NOT CHANGE THIS SETTING THROUGHOUT THE EXPERIMENT.**
4. Now apply this input signal to the circuit you have made keeping the connection to oscilloscope in tact. Feed the output of the circuit to the other channel of oscilloscope. Take care to make all the ground pins common.
5. With input signal amplitude always constant, increase signal frequency slowly. Observe, measure and record the output voltage, V_o . Scan the entire frequency in the range 20 Hz – 2 MHz. You may have to measure V_i and take the ratio V_o/V_i each time in case input fluctuation is too large to hold constant.
6. Calculate the voltage gain for each frequency. Observe the inverted output.
7. Plot the frequency response curve, i.e. voltage gain in dB versus frequency on a semi-log graph-sheet.
8. Estimate the mid-frequency gain and also the lower and higher cut off frequencies and hence the bandwidth.

Observations:

$\beta =$ _____
 $R_1 =$ _____, $R_2 =$ _____, $R_C =$ _____, $R_E =$ _____; $C_1 =$ _____, $C_2 =$ _____, $C_E =$ _____

Table 1: D.C. analysis of the circuit

$$V_{CC} = 12V$$

| Parameter | Computed value | Observed value |
|---------------------------|----------------|----------------|
| V_B (V) | | |
| V_E (V) | | |
| $I_C \approx I_E$ (mA) | | |
| V_{CE} (V) | | |

Q-point is at (__ V, __ mA)

Table 2: Frequency response

$$V_i(\text{pp}) = \text{__ mV}$$

| Sl. No. | Frequency, f (kHz) | $V_o(\text{pp})$ (Volt) | Gain, $A_v = \frac{V_o(\text{pp})}{V_i(\text{pp})}$ | Gain (dB) |
|---------|--------------------|-------------------------|---|-----------|
| 1 | | | | |
| 2 | | | | |
| .. | | | | |
| .. | | | | |

Calculations: $r_e = \text{__}$, $Z_i = \text{__}$, $Z_o = \text{__}$

Theoretical value of A_v in mid-frequency range = __

Graphs: Plot the frequency response curve (semi-log plot) and determine the cut-off frequencies, bandwidth and mid-frequency gain.

Discussions:

Precautions:

1. Vary the input signal frequency slowly.
2. Connect electrolytic capacitors carefully.

Reference: Electronic devices and circuit theory, Robert L. Boylestad & Louis Nashelsky (10th Edition)
